Claims

[1] 【Claim 1】

A chip design verification apparatus, comprising:

at least one hardware block; and

a processing means including at least one software block of performing data communication with the hardware block, and verifying an operation between the hardware block and the software block, the processing means including,

an interface means of transmitting output data of the hardware block, determining whether the output data of the software block is valid, and applying only the valid output data of the software block to the hardware block;

a storage means of storing a software block and a chip design verification program for verifying the software block; and

a controller of transmitting the output data of the software block generated by the operation of executing the chip design verification program to the interface means, determining whether the output data of the hardware block input via the interface means is valid, and applying only the valid output data of the hardware block to the software block.

【Claim 2】

The chip design verification apparatus according to claim 1, wherein the chip design verification program has a graphic user interface, and allows data transceived by executing the chip design verification program to be displayed via the graphic user interface.

【Claim 3】

The chip design verification apparatus according to claim 1, wherein the chip design verification program obtains a multi clock setting value for operating the software block and the hardware block, and stores the value in the interface means.

【Claim 4】

The chip design verification apparatus according to claim 3, wherein the interface means has a clock controller of generating multi clocks in response to the multi clock setting value and a system clock of the interface means and applying the multi clocks to the hardware block.

【Claim 5】

The chip design verification apparatus according to claim 4, wherein the output data of the hardware block has an output value of the hardware block changed in response to the multi clocks applied from the interface means, and a system clock count value of the interface means when the output value of the hardware

block is changed.

【Claim 6】

The chip design verification apparatus according to claim 5, wherein the valid output data of the hardware block is an output value of the hardware block when the system clock count value of the interface means is equal to or smaller than the system clock count value of the chip design verification program, and is an output value of the hardware block when the output value of the software block is not changed even when the system clock count value of the chip design verification program is increased so as to be equal to the system clock count value of the interface means after determination that the system clock count value of the interface means is greater than the system clock count value of the chip design verification program.

【Claim 7】

The chip design verification apparatus according to claim 3, wherein the chip design verification program generates multi clocks in response to the multi clock setting value and the system clock of the chip design verification program to apply the multi clock to the software block.

【Claim 8】

The chip design verification apparatus according to claim 7, wherein output data of the software block has an output value of the software block changed in response to the multi clocks applied from the chip design verification program, and a system clock count value of the chip design verification program when the output value of the software block is changed.

【Claim 9】

The chip design verification apparatus according to claim 8, wherein the valid output data of the software block is an output value of the software block when the system clock count value of the chip design verification program is equal to or smaller than the system clock count value of the interface means, and is an output value of the software block when the output value of the hardware block is not changed even when the system clock count value of the interface means is increased so as to be equal to the system clock value of the chip design verification program after determination that the system clock count value of the chip design verification program is greater than the system clock count value of the interface means.

【Claim 10】

The chip design verification apparatus according to claim 7, wherein the software block has a test-bench, and the test-bench supplies the multi clock setting value to the chip design verification program and operates in response to

the multi clocks of the chip design verification program instead of the multi clocks owned by the test-bench itself.

【Claim 11】

A chip design verification method for a chip design verification apparatus including at least one hardware block and a processing means, the processing means having at least one software block, a chip design verification program, and a storage means of storing input and output data, and an interface means of interfacing with the software block and the hardware block, the method comprising:

a software side operation step of transmitting output data generated by the operation of the software block to the interface means, determining whether the output data of the hardware block received via the interface means is valid by executing the chip design verification program, and applying only the valid output data of the hardware block to the software block; and

a hardware side operation step of transmitting output data generated by the operation of the hardware block to the software block, determining whether the output data of the software block received is valid by executing the chip design verification program in the interface means, and applying only the valid output data of the software block to the hardware block.

【Claim 12】

The method according to claim 11, further comprising:

a step of allowing the chip design verification program to obtain a multi clock setting value to be provided to the interface means, and generate multi clocks in response to a system clock of the chip design verification program and the multi clock setting value to be applied to the software block; and

a step of allowing the interface means to generate multi clocks in response to the system clock of the interface means and the multi clock setting value to be applied to the hardware block.

【Claim 13】

The method according to claim 12, wherein the output data of the hardware block has an output value of the hardware block changed in response to the multi clocks applied from the interface means, and a system clock count value of the interface means when the output value of the hardware block is changed.

【Claim 14】

The method according to claim 13, wherein the valid output data of the hardware block is an output value of the hardware block when the system clock count value of the interface means is equal to or smaller than the system clock count value of the chip design verification program, and is an output value of the

hardware block when the output value of the software block is not changed even when the system clock count value of the chip design verification program is increased so as to be equal to the system clock count value of the interface means after determination that the system clock count value of the interface means is greater than the system clock count value of the chip design verification program.

【Claim 15】

The method according to claim 14, wherein output data of the software block has an output value of the software block changed in response to the multi clocks applied from the chip design verification program, and a system clock count value of the chip design verification program when the output value of the software block is changed.

【Claim 16】

The method according to claim 15, wherein the valid output data of the software block is an output value of the software block when the chip design verification program is equal to or smaller than the system clock count value of the interface means, and is an output value of the software block when the output value of the hardware block is not changed even when the system clock count value of the interface means is increased so as to be equal to the system clock value of the chip design verification program after determination that the system clock count value of the chip design verification program is greater than the system clock count value of the interface means.

【Claim 17】

The method according to claim 16, wherein the software side operation step includes:

a step of initiating an operation of receiving output data of the hardware via the interface means by executing the chip design verification program;

a step of confirming that the valid output data of the hardware block is received and inputting the output data to the software block, when the received system clock count value of the interface means is equal to or smaller than the system clock count value of the chip design verification program, or when the output value of the software block is not changed even when the received system clock count value of the interface means is greater than the system clock count value of the chip design verification program to cause the system clock count value of the chip design verification program to be increased so as to be equal to the received system clock count value of the interface means;

a step of transmitting the output data of the software block to the interface means when the output value of the software block is changed before the system clock

count value of the chip design verification program is increased so as to be equal to the received system clock count value of the interface means; and

a step of initializing the increased system clock count value of the chip design verification program when the input step or the transmission step is completed, and increasing the system clock count value of the chip design verification program while monitoring whether the output value of the software block is changed.

【Claim 18】

The method according to claim 17, wherein the input step includes:

a step of inputting the received output value of the hardware block to the software block as the valid output data of the hardware block when the received system clock count value of the interface means is equal to or smaller than the system clock count value of the chip design verification program;

a step of increasing the system clock count value of the chip design verification program while confirming whether the output value of the software block is changed when the received system clock count value of the interface means is greater than the system clock count value of the chip design verification program; and

a step of inputting the received output value of the hardware block to the software block as the valid output data of the hardware block when the output value of the software block is not changed until the increased system clock count value of the chip design verification program is greater than the received system clock count value of the interface means.

【Claim 19】

The method according to claim 18, wherein the input step further includes:

a step of displaying the valid output data of the hardware block by executing the chip design verification program.

【Claim 20】

The method according to claim 17, wherein the transmission step includes:

a step of increasing the system clock count value of the chip design verification program while confirming whether the output value of the software block is changed, when the received system clock count value of the interface means is greater than the system clock count value of the chip design verification program; and

a step of transmitting the output data of the software block to the interface means when the output value of the software block is changed in the case that the increased system clock count value of the chip design verification program is equal to or smaller than the received system clock count value of the interface

means.

【Claim 21】

The method according to claim 20, wherein the transmission step further includes:

a step of displaying the valid output data of the software block by executing the chip design verification program.

【Claim 22】

The method according to claim 12, wherein the software block has a test-bench, and the test-bench supplies the multi clock setting value to the chip design verification program and operates in response to the multi clocks of the chip design verification program instead of the multi clocks owned by the test-bench itself.

【Claim 23】

The method according to claim 16, wherein the hardware side operation step includes:

a step of initiating an operation of receiving output data of the software via the interface means by executing the chip design verification program;

a step of confirming that the valid output data of the software block is received and inputting the output data to the hardware block, when the received system clock count value of the chip design verification program is equal to or smaller than the system clock count value of the interface means, or when the output value of the interface means is not changed even when the received system clock count value of the chip design verification program is greater than the system clock count value of the interface means to cause the system clock count value of the interface means to be increased so as to be equal to the received system clock count value of the chip design verification program;

a step of transmitting the output data of the hardware block to the chip design verification program when the output value of the hardware block is changed before the system clock count value of the interface means is increased so as to be equal to the received system clock count value of the chip design verification program; and

a step of initializing the increased system clock count value of the interface means when the input step or the transmission step is completed, and increasing the system clock count value of the interface means while monitoring whether the output value of the hardware block is changed.

【Claim 24】

The method according to claim 23, wherein the input step includes:

a step of inputting the received output value of the software block to the hardware block as the valid output data of the software block when the received

system clock count value of the chip design verification program is equal to or smaller than the system clock count value of the interface means;
a step of increasing the system clock count value of the interface means while confirming whether the output value of the hardware block is changed when the received system clock count value of the chip design verification program is greater than the system clock count value of the interface means; and
a step of inputting the received output value of the software block to the hardware block as the valid output data of the software block when the output value of the hardware block is not changed until the increased system clock count value of the interface means is greater than the received system clock count value of the chip design verification program.

【 Claim 25 】

The method according to claim 24, wherein the transmission step includes:
a step of increasing the system clock count value of the interface means confirming whether the output value of the hardware block is changed, when the received system clock count value of the chip design verification program is greater than the system clock count value of the interface means; and
a step of transmitting the output data of the hardware to the chip design verification program when the output value of the hardware block is changed in the case that the increased system clock count value of the interface means is equal to or smaller than the received system clock count value of the chip design verification program.

【 Claim 26 】

A chip design verification method for a chip design verification apparatus including a hardware block and a software block having at least one function block, a chip design verification program for verifying operations of the software block and the hardware block, a storage means of storing input and output data of the software block generated by executing the chip design verification program, and an interface means of performing an interfacing operation between the hardware block and the software block, the method comprising:
a clock generation step of allowing the chip design verification program to obtain a multi clock setting value to be provided to the interface means, and generate multi clocks in response to a system clock of the chip design verification program and the multi clock setting value to be applied to the software block, and allowing the interface means to generate multi clocks in response to the system clock of the interface means and the multi clock setting value to be applied to the hardware block;
a software side operation step of transmitting output data generated by the

operation of the software block operating in response to the multi clocks of the chip design verification program to the interface means, determining whether the output data of the hardware block received via the interface means is valid by executing the chip design verification program, and applying only the valid output data of the hardware block to the software block; and

a hardware side operation step of transmitting output data generated by the operation of the hardware block operating in response to the multi clocks of the interface means to the software block, determining whether the output data of the software block received is valid by executing the chip design verification program in the interface means, and applying only the valid output data of the software block to the hardware block.

【 Claim 27 】

The method according to claim 26, wherein the output data of the hardware block has an output value of the hardware block changed in response to the multi clocks applied from the interface means, and a system clock count value of the interface means when the output value of the hardware block is changed.

【 Claim 28 】

The method according to claim 27, wherein the valid output data of the hardware block is an output value of the hardware block when the system clock count value of the interface means is equal to or smaller than the system clock count value of the chip design verification program, and is an output value of the hardware block when the output value of the software block is not changed even when the system clock count value of the interface means is greater than the system clock count value of the chip design verification program to cause the system clock count value of the chip design verification program to be increased so as to be equal to the system clock count value of the interface means.

【 Claim 29 】

The method according to claim 28, wherein output data of the software block has an output value of the software block changed in response to the multi clocks applied from the chip design verification program, and a system clock count value of the chip design verification program when the output value of the software block is changed.

【 Claim 30 】

The method according to claim 29, wherein the valid output data of the software block is an output value of the software block when the chip design verification program is equal to or smaller than the system clock count value of the interface means, and is an output value of the software block when the output value of the hardware block is not changed even when the system clock count value of the

chip design verification program is greater than the system clock count value of the interface means to cause the system clock count value of the interface means to be increased so as to be equal to the system clock count value of the chip design verification program.

【Claim 31】

The method according to claim 30, wherein the software side operation step includes:

a step of initiating an operation of receiving output data of the hardware via the interface means by executing the chip design verification program;

a step of confirming that the valid output data of the hardware block is received and inputting the output data to the software block, when the received system clock count value of the interface means is equal to or smaller than the system clock count value of the chip design verification program, or when the output value of the software block is not changed even when the received system clock count value of the interface means is greater than the system clock count value of the chip design verification program to cause the system clock count value of the chip design verification program to be increased so as to be equal to the received system clock count value of the interface means;

a step of transmitting the output data of the software block to the interface means when the output value of the software block is changed before the system clock count value of the chip design verification program is increased so as to be equal to the received system clock count value of the interface means; and

a step of initializing the increased system clock count value of the chip design verification program when the input step or the transmission step is completed, and increasing the system clock count value of the chip design verification program while monitoring whether the output value of the software block is changed.

【Claim 32】

The method according to claim 31, wherein the input step includes:

a step of inputting the received output value of the hardware block to the software block as the valid output data of the hardware block when the received system clock count value of the interface means is equal to or smaller than the system clock count value of the chip design verification program;

a step of increasing the system clock count value of the chip design verification program while confirming whether the output value of the software block is changed when the received system clock count value of the interface means is greater than the system clock count value of the chip design verification program; and

a step of inputting the received output value of the hardware block to the software block as the valid output data of the hardware block when the output value of the software block is not changed until the increased system clock count value of the chip design verification program is greater than the received system clock count value of the interface means.

【 Claim 33 】

The method according to claim 32, wherein the input step further includes:

a step of displaying the valid output data of the hardware block by executing the chip design verification program.

【 Claim 34 】

The method according to claim 31, wherein the transmission step includes:

a step of increasing the system clock count value of the chip design verification program while confirming whether the output value of the software block is changed, when the received system clock count value of the interface means is greater than the system clock count value of the chip design verification program; and

a step of transmitting the output data of the software block to the interface means when the output value of the software block is changed in the case that the increased system clock count value of the chip design verification program is equal to or smaller than the received system clock count value of the interface means.

【 Claim 35 】

The method according to claim 34, wherein the transmission step further includes:

a step of displaying the valid output data of the software block by executing the chip design verification program.

【 Claim 36 】

The method according to claim 26, wherein the software block has a test-bench, and the test-bench supplies the multi clock setting value to the chip design verification program and operates in response to the multi clocks of the chip design verification program instead of the multi clocks owned by the test-bench itself.

【 Claim 37 】

The method according to claim 30, wherein the hardware side operation step includes:

a step of initiating an operation of receiving output data of the software block via the interface means by executing the chip design verification program;

a step of confirming that the valid output data of the software block is received and inputting the output data to the hardware block, when the received system

clock count value of the chip design verification program is equal to or smaller than the system clock count value of the interface means, or when the output value of the interface means is not changed even when the received system clock count value of the chip design verification program is greater than the system clock count value of the interface means to cause the system clock count value of the interface means to be increased so as to be equal to the received system clock count value of the chip design verification program;

a step of transmitting the output data of the hardware block to the chip design verification program when the output value of the hardware block is changed before the system clock count value of the interface means is increased so as to be equal to the received system clock count value of the chip design verification program; and

a step of initializing the increased system clock count value of the interface means when the input step or the transmission step is completed, and increasing the system clock count value of the interface means while monitoring whether the output value of the hardware block is changed.

【Claim 38】

The method according to claim 37, wherein the input step includes:

a step of inputting the received output value of the software block to the hardware block as the valid output data of the software block when the received system clock count value of the chip design verification program is equal to or smaller than the system clock count value of the interface means;

a step of increasing the system clock count value of the interface means while confirming whether the output value of the hardware block is changed when the received system clock count value of the chip design verification program is greater than the system clock count value of the interface means; and

a step of inputting the received output value of the software block to the hardware block as the valid output data of the software block when the output value of the hardware block is not changed until the increased system clock count value of the interface means is greater than the received system clock count value of the chip design verification program.

【Claim 39】

The method according to claim 37, wherein the transmission step includes:

a step of increasing the system clock count value of the chip design verification program while confirming whether the output value of the hardware block is changed, when the received system clock count value of the chip design verification program is greater than the system clock count value of the interface means; and

a step of transmitting the output data of the hardware to the chip design verification program when the output value of the hardware block is changed in the case that the increased system clock count value of the interface means is equal to or smaller than the received system clock count value of the chip design verification program.